23. The semiconductor processing method of claim 21, wherein the threshold voltages for the two series of field effect transistors are defined by a common channel implant, said implant being the only channel implant which defines the threshold voltages for the two series of field effect transistors.

24. The semiconductor processing method of claim 21, wherein the threshold voltages for the two series of field effect transistors are defined by one or more common channel implants.

25. The semiconductor processing method of claim 21, wherein the threshold voltages for the two series of field effect transistors are defined by one or more common channel implants, said common channel implants being the only channel implants which define the threshold voltages for the two series of field effect transistors.

26. A semiconductor processing method comprising forming two series of field effect transistors over a substrate, at least one series being isolated from adjacent devices by shallow trench isolation, and further comprising achieving different threshold voltages between field effect transistors in different series by varying the active area widths of the field effect transistors in the series, at least one series having active area widths less than one micron.

27. The semiconductor processing method of claim 26, wherein the threshold voltages for the two series of field effect transistors are defined by a common channel implant.

28. The semiconductor processing method of claim 26, wherein the threshold voltages for the two series of field effect transistors are defined by a common channel implant, said implant being the only channel implant which defines the threshold voltages for the two series of field effect transistors.

29. The semiconductor processing method of claim 26, wherein the threshold voltages for the two series of field effect transistors are defined by one or more common channel implants.

30. The semiconductor processing method of claim 26, wherein the threshold voltages for the two series of field effect transistors are defined by one or more common channel implants, said common channel implants being the only channel implants which define the threshold voltages for the two series of field effect transistors.

N w Claims

51. A semiconductor processing method comprising forming two series of field effect transistors over a substrate, one series being isolated from adjacent devices by shallow trench isolation, the other series having active area widths greater than one micron, the one series being formed to have active area widths less than one micron to achieve lower threshold voltages than the other of the series, wherein the threshold voltages for the two series of field effect transistors are defined by a shared channel implant.

52. The semiconductor processing method of claim 51, wherein all threshold voltages of the two series of field effect transistors are less than two volts.

53. The semiconductor processing method of claim 51, wherein the threshold voltages for the two series of field effect transistors are defined by the shared channel implant, said implant being the only channel implant defining the threshold voltages for the two series of field effect transistors.

54. The semiconductor processing method of claim 51, wherein the threshold voltages for the two series of field effect transistors are defined by one or more shared channel implants.

55. The semiconductor processing method of claim 51, wherein the threshold voltages for the two series of field effect transistors are defined by one or more shared channel implants, said shared channel implants being the only channel implants defining the threshold voltages for the two series of field effect transistors.

56. A semiconductor processing method comprising forming two series of field effect transistors over a substrate, at least one series being isolated from adjacent devices by shallow trench isolation, and further comprising achieving different threshold voltages between field effect transistors in different series by varying the active area widths of the field effect transistors in the series, at least one series having active area widths less than one micron, wherein the threshold voltages for the two series of field effect transistors are defined by a shared channel implant.

57. The semiconductor processing method of claim 56, wherein all threshold voltages of the two series of field effect transistors are less than two volts.

58. The semiconductor processing method of claim 56, wherein the threshold voltages for the two series of field effect transistors are defined by the shared channel implant, said implant being the only channel implant which defines the threshold voltages for the two series of field effect transistors.

59. The semiconductor processing method of claim 56, wherein the threshold voltages for the two series of field effect transistors are defined by one or more shared channel implants.

60. The semiconductor processing method of claim 56, wherein the threshold voltages for the two series of field effect transistors are defined by one or more shared channel implants, said shared channel implants being the only channel implants which define the threshold voltages for the two series of field effect transistors.